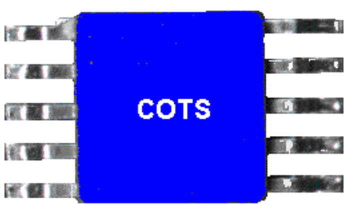
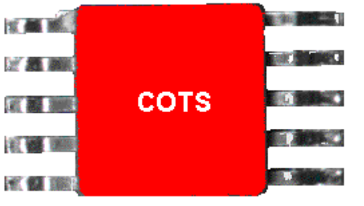
Military & Aerospace /Avionics COTS Conference

August 22-25, 2000

Commercial Off-The-Shelf (COTS) Program

Methodology and Results of Upscreening Electronic Parts - An Update





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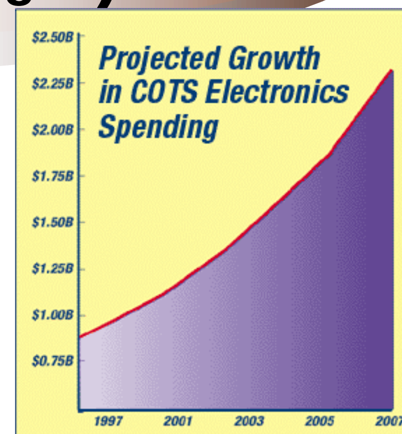
AGENDA:

- ADVOCACY FOR COTS
- DRAWBACKS WHEN IMPLEMENTING COTS
- JPL COTS^{++} CRITICAL SCREENING FLOW
- JPL COTS^{++} CRITICAL QUALIFICATION
- COST & SCHEDULE TRADEOFFS
- COTs++ Upscreening Results
- C-SAM Update and Ongoing Work
- COTS DPA Failures
- SUMMARY

Advocacy for Using COTS(plastic packages):



Military & Aerospace Publication

1. State of-the-art parts are mostly available as COTS

2. COTS plastic parts performance capabilities continue to increase (e.g. processing power & high density memories)

3. COTS plastic parts enable reduction of hardware weight and volume

4. COTS plastic parts initial acquisition cost is less than ceramic

5. COTS plastic parts have been reported to demonstrate good to excellent reliability in commercial and aerospace applications

6. Often they are the only option when Space level part is not offered or available

EPE 5-14

Drawback to COTS Implementation (plastic packages):

1. Upscreening cost is coupled to the following influences and therefore cannot be tightly controlled (no standard exists)
   - Finding suitable test expertise
   - Minimum quantities often dictate cost
   - Manufactures unwillingness to upscreen
   - Costs of ownership depends on risk accepted

2. Upscreening schedules can jeopardize project schedules unless
   - Flows and processes are in writing & approved
   - Engineering/QA help is available daily
   - Vendor commits to screening schedule
   - Material in-process status is monitored weekly

3. Risk is not totally eliminated with upscreening

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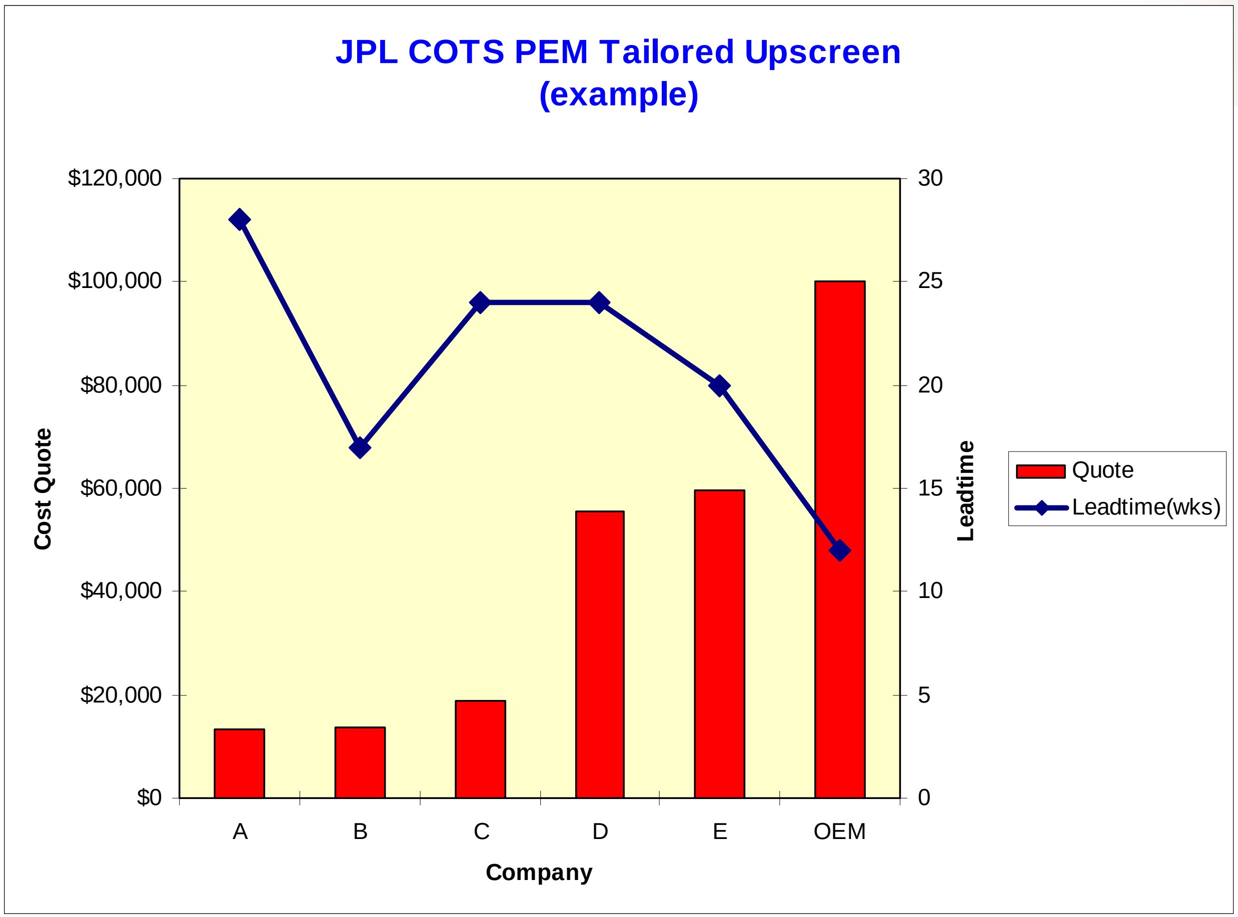
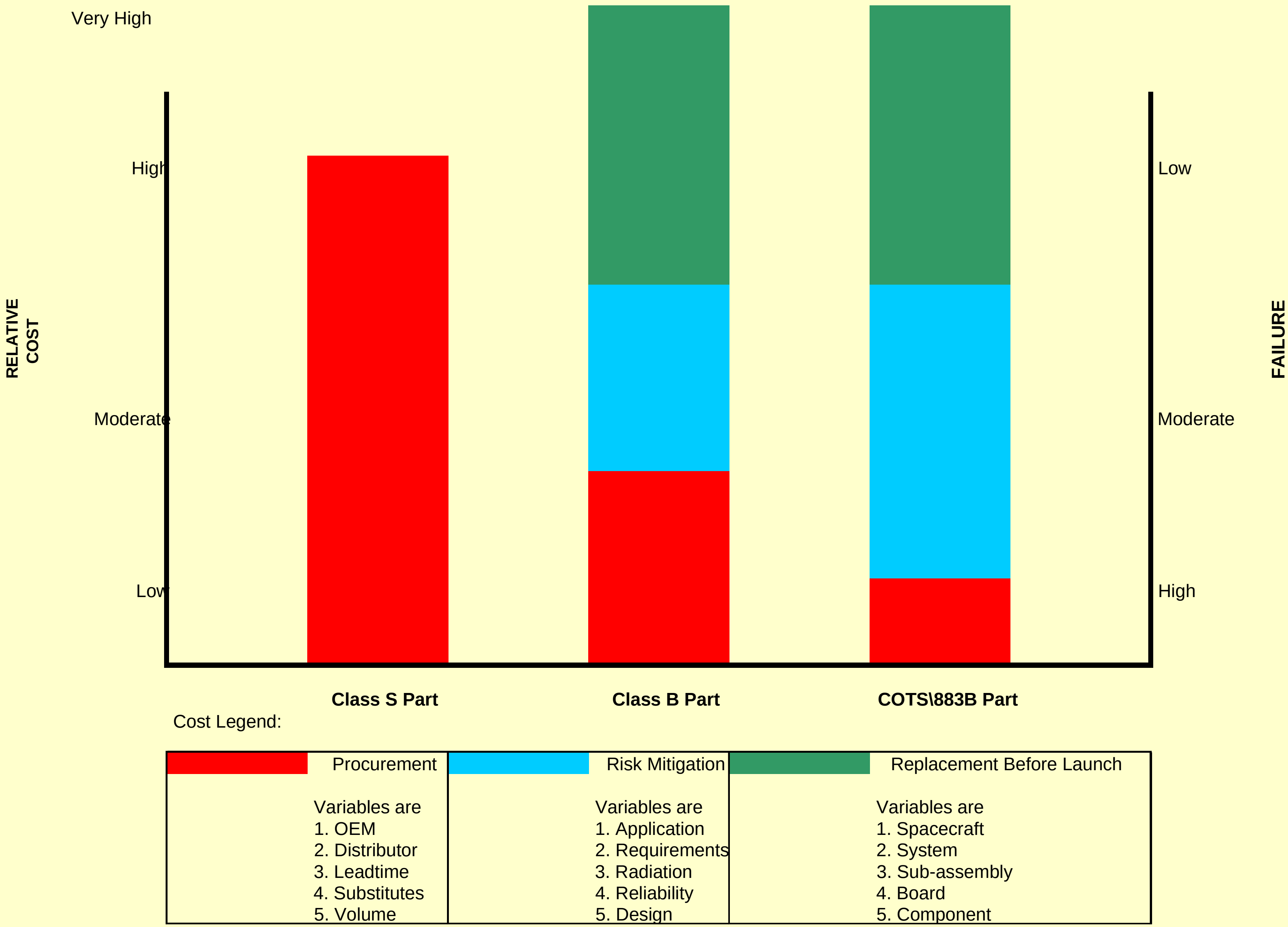


Competitive bidding demonstrates cost & schedule selection tradeoffs

Likelihood of Part Failure Vs Cost for Space Flight Applications

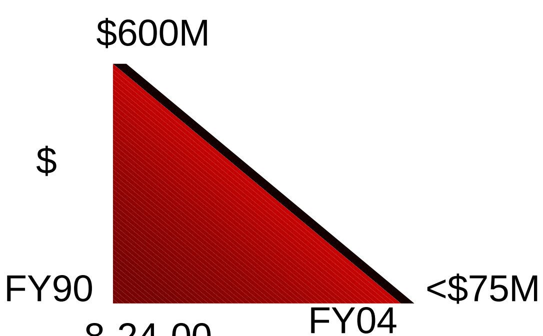


More Risk Management is Needed:

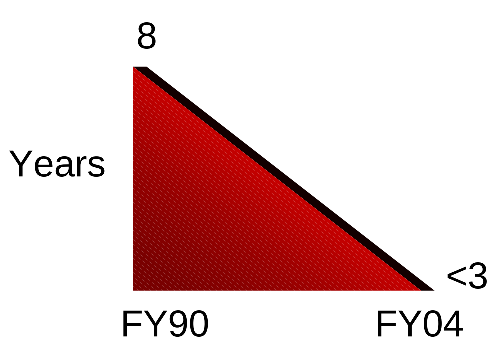
JPL/NASA Project Drivers:

- Must infuse the latest technology
- Must significantly reduce development costs
- Must significantly reduce development time
- Per NASA, Better, Faster, Cheaper is here to stay

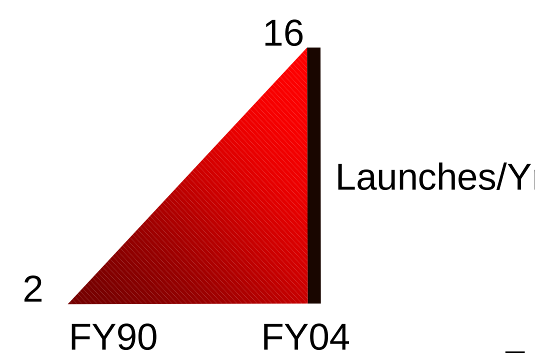
Average Development Costs



Average Development Time



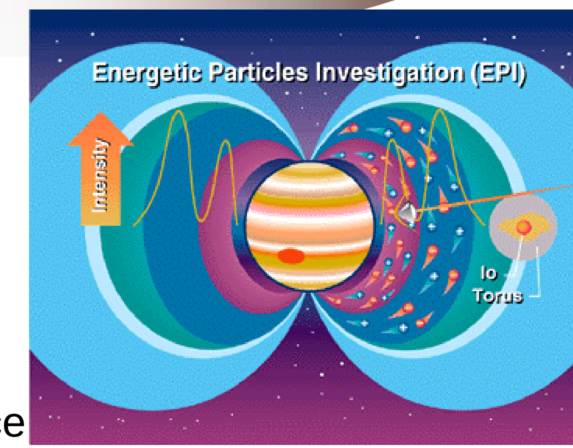
Average Flight Rate



COTS PEM Risk Mitigation Addresses the Following Concerns:

- **Narrow Temperature Range for Commercial Grade**
- **Plastic Assembly Quality**
- **Lot Non-Uniformity & Traceability (including radiation)**
- **Adequacy of Vendors Testing**
- **Infant Mortality**
- **Die Construction and Quality**

Radiation Issues of Using COTS for Space Applications:



Rad Hard Assurance Varies from the same processing lot

Radiation Assurance has little statistical confidence

TID response depends on process-

"Positive" process changes can reduce radiation tolerance

SEE depends on circuit design and dimensions-

Commercial vendor can change these without notice

No good way of predicting radiation response without extensive testing-

Exception is a controlled Rad Hard process line

Radiation risk mitigation techniques are often required- $$$

Methods to Insure Low Risk COTS in Critical Space Applications

Proposed Target Guidelines

15 yr mission:	JPL Upscreen/ Qual	+	Derate/WLA/ RLAT/DPA/QML
10 yr mission:	JPL Upscreen/ Qual	+	Derate/WLA/ RLAT/DPA/QML
5 yr mission:	JPL Upscreen/ Qual	+	Derate/ RLAT/DPA/QML
1 yr mission:	JPL Upscreen	+	DPA/Generic Data

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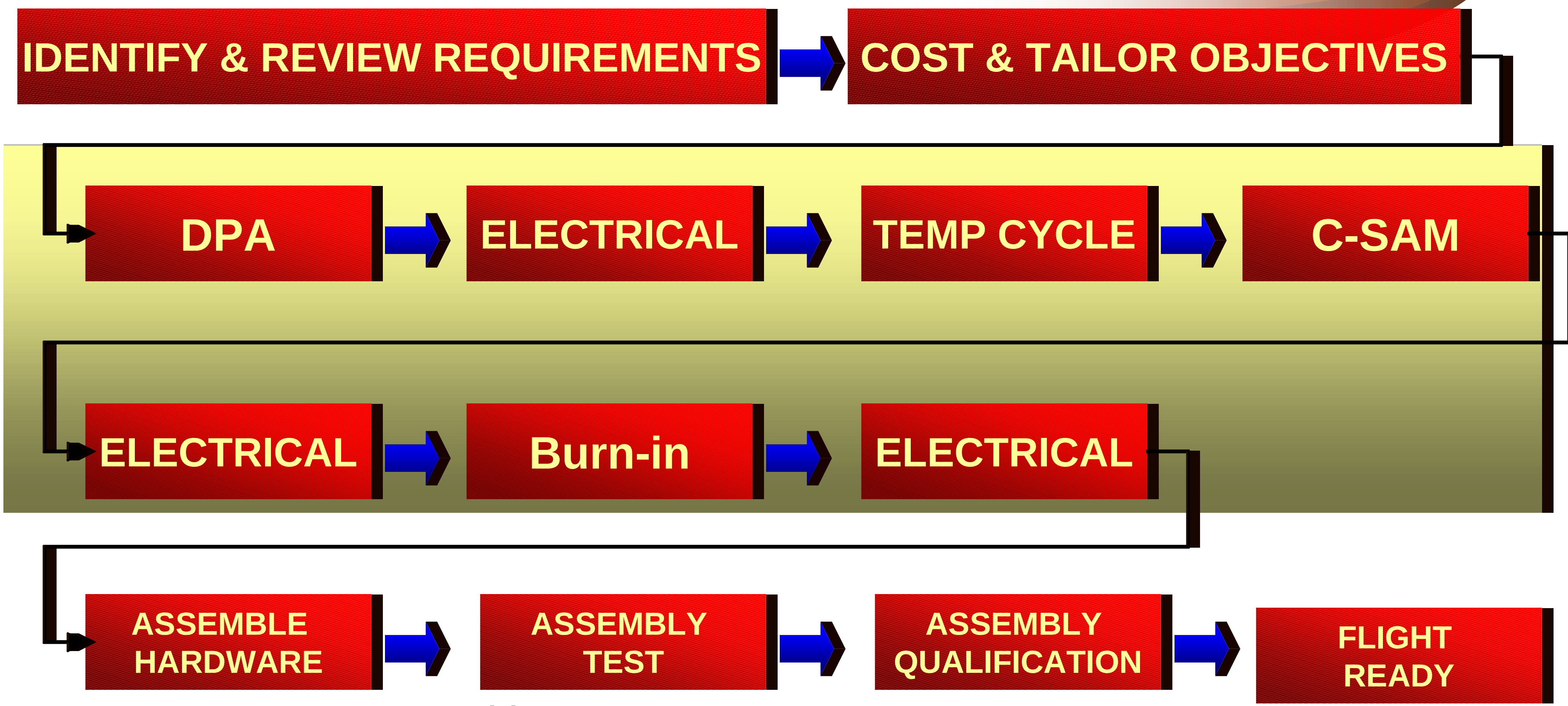
Part Level Screening



COTS^{++} Plastic Infusion Critical Screening Flow
(Tailored for Project application/mission requirements)

Part/ Lot Qualification

IDENTIFY & REVIEW REQUIREMENTS → COST & TAILOR OBJECTIVES

RADIATION → OUTGASSING → HUMIDITY → T-CYCLE

DPA → LIFE TEST → RLAT

DATA REVIEW → RISK RATING → RISK MITIGATION → FLIGHT ACCEPTANCE

COTS^{++} Plastic Infusion Critical Qualification
(Tailored for Project application/mission requirements)

COTS^{++} PEM Upscreen Impact on Risk Mitigation:

	Amplifier	ADC	DC-DC Conv.	Reg.
• Narrow Temp.Range for Commercial Grade	1	1	3	9
• Plastic Assembly Quality	3	9	9	1
• Lot Non- Uniformity & Traceability	1	9	3	3
• Adequacy of Vendors Testing	1	9	3	9
• Infant Mortality	1	9	1	9
• Die Construction and Quality	1	1	1	1
Total Score	8	38	20	31
COTS^{++} Impact on Lowering Risk	Low	High	High	High
Fallout	4%	65%	26%	25%

Risk mitigation weighting factors used: Minimum = 1, Moderate = 3, Significant = 9

COTS^{++} Upscreening Rejects by Part Type & Vendor

	Amplifier- A	ADC- B	ADC2-B	DC-DC Con.-C	Voltage C-A	S.Regulator-B
DPA:	0/4	1/8	TBD	0/4	0/4	0/4
Incoming:	0/78	n/a	4/79	1/78	0/80	8/80
C-SAM:	3/78	38/78	9/75	16/77	5/80	0/80
Temp Cycle:	0/78	10/78	0/75	3/77	0/80	3/72
Burn-In:	0/78	3/68	0/75	0/74	0/80	9/69
QCI:	0/10	0/10	0/10	0/10	0/10	0/10
Total:	3/78	51/78	TBD	20/78	5/80	20/80

Failure Mechanisms from PEM Delamination:

• Stress-induced passivation damage over the die surface

• Wire bond degradation due to shear displacement

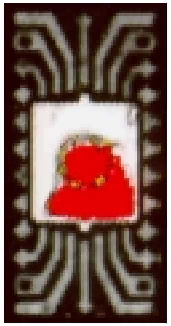
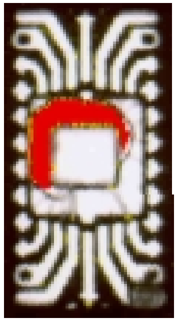
• Accelerated metal corrosion

• Die attach adhesion

• Intermittent electricals at high temperature

• Popcorn cracking

• Die cracking

CSAM Yields
06/12/2000

Part Type	Manufacturer	Yield
NPN Transistor 1	A	83%
Switching Diode	A	0%
NPN Transistor 2	A	100%
Zener Diode	A	50%
NPN Transistor 3	A	100%
Op-Amp 1	B	87%
Op-Amp 2	C	0%
Op-Amp 3	C	7%
Phase Detector	D	100%
MMIC	E	40%

Results are package/ vendor assembly dependent

Lot sizes range from 15-30 parts each.

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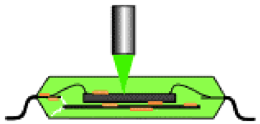
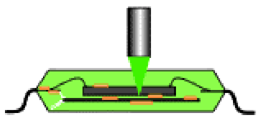
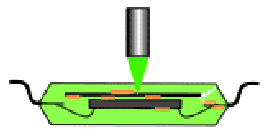
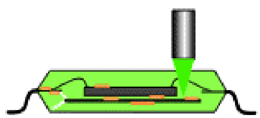
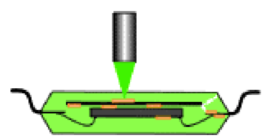
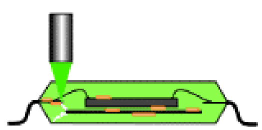
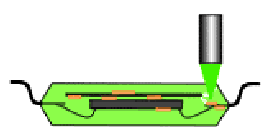
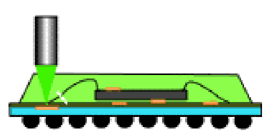
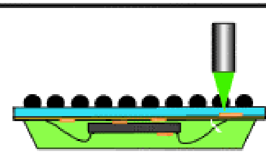
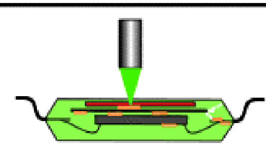
	Circuit Side Scan	Non-Circuit Side Scan
Type I Delamination: Encapsulant/Die Surface		
Type II Delamination: Die Attach Region		
Type III Delamination: Encapsulant/Substrate (Die Side)		
Type IV Delamination: Substrate/Encapsulant (Backside)		
Type V Delamination: Encapsulant/Lead Interconnect		
Type VI Delamination: Intra-laminate (Laminate Substrates Only)		
Type VII Delamination: Heat Sink/Substrate		

IC defect descriptions are now identified in J-STD-035

(Acoustic Microscopy for NonHermetic Encapsulated Electronic Components)

Source: Sonoscan Inc.

A New Failure Characterization Study is Underway Utilizing Plastic Part C-SAM Rejects

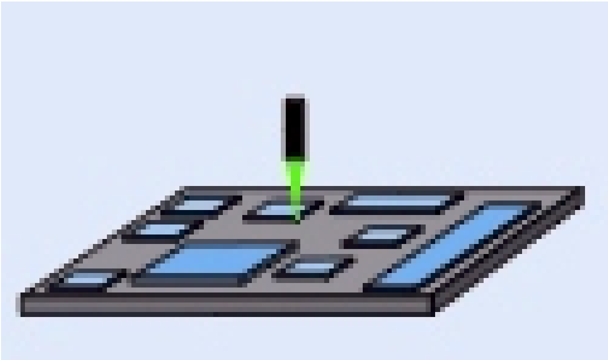
Objectives:

- Identify C-SAM reject parts by criteria(s)
- Measure Material Properties including sonic test, IR, X-ray
- Apply extreme temperature cycle stresses
- Repeat Material Properties Measurements including C-SAM at different intervals
- Identify all failure mechanisms and risk rate C-SAM rejects

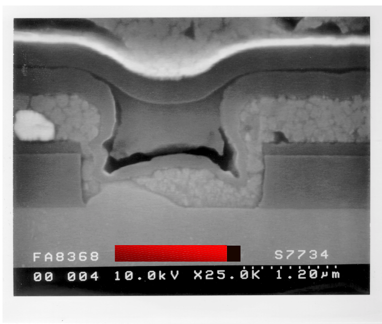
A Failed Chip Scale Board Assembly is under investigation utilizing C-SAM inspection on components/board

Objectives:

- Identify component delaminations
- Identify board layer delaminations
- Make correlation to CSP package thermal cycle failures
    - CTE Mismatch
    - Package Proximity and Location on Board
    - Ball Bond Size and Location



Updated Examples of COTS Parts/Die Failing DPA



A/D

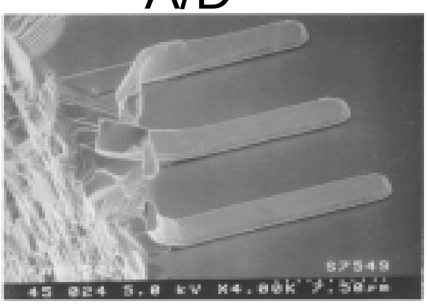
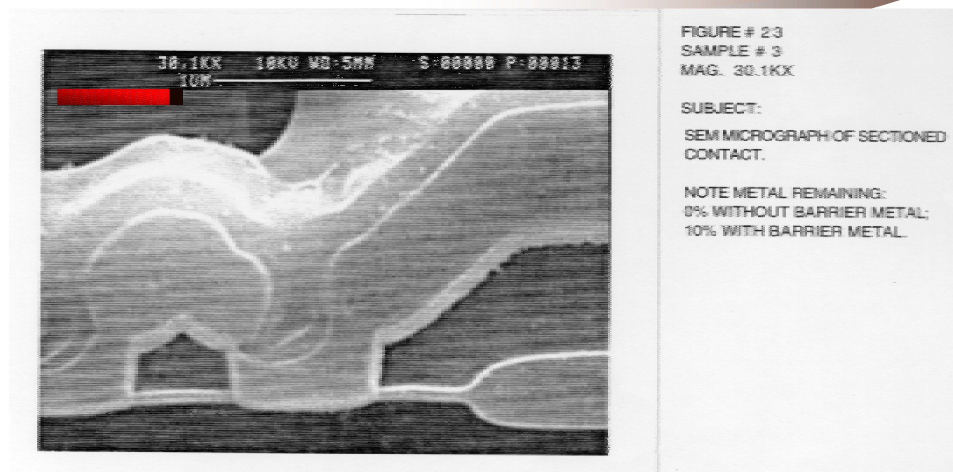


Figure 3. 4,000X SEM micrograph of loosened metallization traces along edge of die.

RF



PROM

Metallization anomalies are
the predominant failures

EPE 514

Summary/Conclusions:

- The concerns/risks anticipated with using COTS PEMS can be reduced to acceptable medium risk levels using JPL upscreening.

- A part qualification plan has been added to JPL's existing screening flows to further insure the reliability of parts used by Projects when application requirements are different.

- Further investigations/studies are being conducted on individual components and board assemblies using C-SAM analysis. This information will provide more understanding of the correlation between delamination and component/ board failure mechanisms.

Visit JPL COTS Web Site at

http://cots.jpl.nasa.gov/